

REMARKS

Status of the Claims

Applicants request the Examiner to reconsider the application as amended. Claims 1-16 are pending. Claims 17-32 have been canceled. Claims 1-5, 8, 10, 12 and 16 have been rejected. Claims 6-7, 9, 11, and 13-15 have been objected to as being dependant upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. (Final Office Action, page 3). Applicants wish to express appreciation to the Examiner for the indication of allowable subject matter.

Election/Restrictions

The Examiner noted in the Final Office Action that “[t]his application contains claims 17-32 drawn to an invention nonelected without traverse in Paper No. 042605. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action” (Final Office Action, page 2). Applicants have canceled claims 17-32. Applicants further assert the right to present these claims in a divisional application claiming the benefit of the present application.

Rejection of Claims 1-5, 8, 10, 12, and 16 Under 35 U.S.C. § 102(a) in view of Mitsuhashi

Claims 1-5, 8, 10, 12, and 16 were rejected under 35 U.S.C. § 102(a) as allegedly being anticipated by U.S. Published Application No. 2003/0104706 to Mitsuhashi et al. (“Mitsuhashi”). Applicants have submitted, in their previous Amendment and Response, that Mitsuhashi does not teach a thinning process on a high-k dielectric material and then,

following this thinning process, forming a conductive gate structure on the ultrathin high-k dielectric. Instead, Mitsuhashi teaches forming a gate electrode structure prior to its disclosed thinning process. *See, e.g.,* Mitsuhashi, page 2, paragraph [0022] (“a third step of patterning the conductive film so as to form a gate electrode . . . a fifth step of removing, by wet-etching, the exposed portion of the metal oxide film . . .”).

The Examiner responded by maintaining that Mitsuhashi does “teach thinning the high-k dielectric layer prior to formation of a gate electrode structure.” (Final Office Action, page 4). According to the Examiner, “as noted in paragraph [0055] of Mitsuhashi et al., an anneal process is performed which compacts the hafnium oxide layer. As noted in table 1 of the Ng et al. reference cited in the previous office action (mentioned here as a teaching reference) hafnium oxide decreases in thickness (i.e. is thinned) with thermal annealing.” (*Id.*)

In response to the Examiner, Applicants submit that any incidental decrease in thickness of an HfO_2 film that may result from a thermal annealing process would not be understood by persons of skill in the art as “a thinning process” as recited in claim 1 of the present application. Instead, applicants submit that a person having ordinary skill in the art would understand “a thinning process” to include removal of at least a portion the layer or material to be thinned. *See, in this regard, Mitsuhashi paragraphs [0025-0026]:*

Moreover, in the first method for manufacturing a semiconductor device, it is preferred that the third step includes a step of successively plasma-etching the conductive film and the metal oxide film by using a mask pattern that covers a gate electrode formation region so as to *thin* the portion of the metal oxide film that is located outside the gate electrode.

In this way, the unnecessary portion of the metal oxide film is *thinned* so that the damaged layer can be formed entirely across the unnecessary,

portion, whereby the unnecessary portion can be completely *removed* by wet-etching.

(Emphasis added).

Applicants further direct the Examiner to the specification of the present application, which states examples of thinning processes falling within the scope of the invention. Such processes include wet etching, dry etching, and hybrid damage/wet etching processes. (*See, e.g.*, Applicants' Specification, page 5, second paragraph; and pages 9-11). Such processes would necessarily involve removal of at least some of the layer or material to be thinned. (*See, e.g.*, Applicants' Specification, page 5, second paragraph; page 8, first paragraph; page 9, first full paragraph; page 9, third paragraph; page 13, Example 1; page 13, Example 2; and page 14, Example 3). In addition, such thinning processes are recited as being a separate processing step from annealing (*See, e.g.*, Applicants' Specification, page 7, third full paragraph; page 8, second and third paragraphs; page 9, first full paragraph; page 9, third paragraph ("dielectric . . . may be annealed in an inert (or alternatively) a reactive ambient prior to the thinning process.")).

Accordingly, applicants submit that Mitsubishi fails to teach or suggest Applicants' claimed invention for at least the reason that it fails to teach forming a conductive gate structure on said ultrathin high-k dielectric following "a thinning process," as that term would be understood in the art and in Applicants' Specification. Applicants, therefore, submit that claims 1-16 are in immediate condition for allowance.

Conclusion

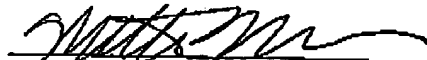
In view of the foregoing, the rejections should be withdrawn and all pending claims should be allowed.

If prosecution may be further advanced, Examiner is invited to telephone the undersigned to discuss this application.

Applicants believe no fees are due in conjunction with the filing of this Amendment. However, if any additional fees are due, such as a fee for a further extension of time, please charge the fees to Deposit Account No. 50-0510.

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Respectfully submitted,


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